IN THE CLAIMS

Presented below is a complete list of claims with changes marked up:

1-19. Canceled.

20. (Currently Amended) The ~~communications network~~system of claim ~~19~~ 42, wherein~~:~~

the first target comprises a first configuration block ~~on an integrated circuit;~~ and

the second target comprises a second configuration block ~~on the integrated circuit~~.

21. Canceled

22. (Currently Amended) The ~~communications network~~system of claim ~~21~~ 42, wherein the configuration ring further ~~comprising~~comprises~~:~~

a second master~~,~~ coupled to the ring ~~coupled to the second master~~.

23. (Currently Amended) The ~~communications network~~system of claim 22, wherein the configuration ring further ~~comprising:~~comprises

an arbitrator, ~~the arbitrator~~ coupled to the ~~first~~ master~~, the arbitrator coupled to~~ and the second master, the arbitrator controlling activity of the ~~first~~ master and the second master.

24. (Currently Amended) The ~~communications network~~system of claim 22, wherein the configuration ring further ~~comprising:~~comprises

a request line~~, the request line~~ coupled to the ~~first~~ master~~, the request line coupled to~~ and the second master; and

a grant line~~, the grant line~~ coupled to the ~~first~~ master~~, the grant line coupled to~~ and the second master.

25. (Currently Amended) The ~~communications network~~system of claim 24, wherein ~~further comprising:~~

the request line is configured to pass signals in a first direction~~,~~ and the grant line is configured to pass signals in a second direction.

26. (Currently Amended) The ~~communications network~~system of claim 25, ~~wherein:~~

the first direction and the second direction are dynamically alterable.

27. (Currently Amended) The ~~communications network~~system of claim 22, wherein the configuration ring further ~~comprising~~comprises:

a request line~~, the request line~~ coupled to the ~~first~~ master, ~~the request line coupled to~~ the second master, ~~the request line coupled to~~ the first target, ~~the request line coupled to~~and the second target.

28. (Currently Amended) The ~~communications network~~system of claim 27, ~~wherein:~~

the request line is configured such that signals on the request line flow in a logically opposite direction to signals on the ring.

29. (Currently Amended) The ~~communications network~~system of claim 28, wherein~~:~~

the ring ~~comprising~~ comprises a grant line and a set of data lines, the grant line is configured to indicate ~~a~~ the master may use the ring, the data lines are configured to transmit signals.

30. Canceled.

31. (Currently Amended) The ~~communications network~~system of claim ~~21~~ 42, wherein~~:~~

the ring ~~comprising~~ comprises a set of data lines~~,~~ and the data lines are configured to transmit signals.

32. (Currently Amended) The ~~communications network~~system of claim 31, wherein~~:~~

the ~~first~~ master ~~utilizing~~ uses the ring to transmit signals to the first target, the first target ~~utilizing~~ uses the ring to transmit signals to the second target, and the second target ~~utilizing~~ uses the ring to transmit signals to the first master.

33. (Currently Amended) The ~~communications network~~system of claim 31, wherein~~:~~

the ~~first~~ master ~~comprising~~ comprises a ring interface coupled to the ring and a control coupled to the ring interface, the control suitable for generating packets, the packets being transmitted through the ring interface to become signals on the ring.

34. (Currently Amended) The ~~communications network~~system of claim 33, wherein: the first target ~~comprising~~ comprises a ring interface and a decoder coupled to the ring interface, the decoder receiving the signals that represent a packet, the decoder determining if the packet is addressed to the first target.

35. (Currently Amended) The ~~communications network~~system of claim 34, wherein: the second target ~~comprising~~ comprises a ring interface and a decoder coupled to the ring interface, the decoder receiving the signals that represent a packet, the decoder determining if the packet is addressed to the second target.

36. (Currently Amended) The ~~communications network~~system of claim 35, wherein: the packet ~~comprised of~~comprises a header and a set of data, the header including an indication of the logical size of the set of data.

37. (Currently Amended) The ~~communications network~~system of claim 35 wherein: the packet comprised of a ~~fixed~~ predetermined number of units of data, the units of data encoding an address.

38-40. Canceled.

41. (Currently Amended) The ~~communications network~~system of claim 22, wherein: the second master ~~comprising~~ comprises a buffer~~, the buffer utilized for storing~~ to store incoming data when the second master originates a packet, the incoming data is passed after the

second master completes origination of the packet.

42. (Previously presented) A system comprising:

a processor;

a processor bus coupled to the processor;

a data chip coupled to the processor bus; and

an address chip coupled to the processor bus and coupled to the data chip, the address chip including a configuration ring, the configuration ring having a master, a first target and a second target, the master coupled through a ring to the first target, the first target coupled through the ring to the second target, the second target coupled through the ring to the master, wherein the master originates a plurality of packets containing configuration information and passes the plurality of packets to the first and second targets via the ring to configure the first and second targets.

43. (Currently Amended) ~~A~~ The system of claim 42, further comprising:

a graphics memory device;

an accelerated graphics port; and

a graphics expander bridge coupled to the graphics memory device and the accelerated graphics port, the graphics expander bridge comprising a plurality of functional blocks and a second ring by which the plurality of functional blocks are coupled to each other, the second ring and the plurality of functional blocks residing on a single integrated circuit chip, each of the plurality of functional blocks having a decoder and a plurality of configuration registers, wherein one of the plurality of functional blocks originates one or more packets containing configuration

information and passes the one or more packets to one or more of the remaining functional blocks via the second ring to configure the one or more of the remaining function blocks.

44. (Currently Amended) The system of claim 43, wherein each of the plurality of functional blocks further comprises a ring interface to couple to the second ring.

45. (Currently Amended) The system of claim 43, wherein the second ring comprises a plurality of data lines to transmit the one or more packets.